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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	6

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,174	LAVELLE ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) 11-32 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

a. System Claims 1-10, computer graphics display memory, for storing condition code, flag or status are Class 345, subclass 556.

b. System Claims 11-16, computer graphics display memory, compressed data transferring and processing graphics data to a frame buffer, are classified in class 345, subclass 530.

c. Method Claims 17-22, computer graphics display memory, plural storage devices, are classified in Class 345, subclass 536.

d. Method Claims 23-29, computer graphics display memory, cache are classified in Class 345, subclass 557.

e. Method Claims 30-32, computer graphics display memory, graphics display memory controller are classified in Class 345, subclass 531.

Applicant is required under 35 U.S.C. 121 to elect a single invention for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the invention that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional inventions which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected inventions. MPEP § 809.02(a).

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

2. On March 2, 2004, a call was made to Mr. Jeffrey C. Hood, telephone number in the PALM database (1-512-853-8800) to request an oral election to the above restriction requirement. Applicant elected Claims 1-10 with traverse.

3. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, and in further view of Jeddeloh, U.S. Patent Application Publication 2003/0070044.

6. Regarding claim 1, Olszewski discloses a graphics system comprising: a memory configured to receive and store graphics data, wherein the memory comprises, a RAM

configured to store the graphics data, a level two cache memory connected to the RAM, and a level one cache memory connected to the level two cache memory (Figure 2B, Column 4, lines 2-3, 38-53); an array of registers configured to store status information, wherein the status information tracks and indicates accesses to the graphics data in the level one cache, wherein the status information (Figure 2B, element 240, 245; Column 5, lines 4-6, 30-45; Figure 4-5, Column 7, lines 1-46); and memory connected to the array of registers (Figure 2B, Column 2, lines 38-64, *frequently accessed memory items, memory accesses,* Column 7, lines 1-46).

Olszewski does not disclose further indicates whether the graphics data is modified or unmodified. Bowles teaches further indicates whether the graphics data is modified or unmodified (Column 3, line 50 through Column 4, line 7; Column 6, lines 6-21). The motivation for combining level one cache information tracking with whether the data has been modified is for reducing the cache memory access or snooping overhead (Column 1, lines 14-18). Bowles is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with whether the data has been modified, as Bowles teaches, to improve cache memory efficiency.

Olszewski discloses memory accesses and register array but does not disclose a memory request processor connected to the memory wherein the memory request processor controls. Jeddeloh teaches a memory request processor connected to the memory wherein the memory request processor controls (Figures 1-2, Page 2, Paragraph 15). The motivation for combining level one cache information tracking, memory requests, and register array with a memory request processor connected to the memory is to reduce memory access latency (Page 1, Paragraph 2;

Page 2, Paragraphs 10-14). Jeddeloh is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines to combine the benefits of level one cache information tracking, memory requests, and register array, as Olszewski discloses, with a memory request processor connected to the memory, as Jeddeloh teaches, is to reduce memory access latency.

Olszewski does not disclose transfer of data from the level one cache memory to the level two cache memory according to the status information. Bowles teaches transfer of data from the level one cache memory to the level two cache memory according to the status information (Column 7, lines 49-60). The motivation for combining level one cache information tracking with transferring data from level 1 to level 2 cache according to status is for reducing the cache memory access or snooping overhead (Column 1, lines 14-18). Bowles is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with transferring data from level 1 to level 2 cache according to status, as Bowles teaches, to improve cache memory efficiency.

Claim Rejections - 35 USC § 103

7. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, Jeddeloh, U.S. Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Longhenry et al, U.S. Patent 5,991,865.

8. Regarding claim 2, representative of claims 3-4, Olszewski discloses a graphics system of claim 1, wherein the data comprises samples (Column 4, lines 2-3; Column 6, lines 45-51).

[further claims 2-4] Olszewski does not disclose comprises graphics samples, pixels, and wherein the level one cache memory is divided into logical blocks, and wherein each register of status information corresponds to one logical block.

Longhenry teaches graphics data as samples, pixels and wherein the level one cache memory is divided into logical blocks, and wherein each register of status information corresponds to one logical block (Column 4, lines 48-67; Column 14, line 49; *"macro block"*, Column 12, lines 48-59). The motivation for combining level one cache information tracking with level one cache divided into logical blocks of graphics data as pixels and samples, and each register of status information corresponds to one logical block is that multimedia decompression using vectorized real time video data and MPEG standards requires logical blocks of adjacent pixels and sample interpolation (Column 1, line 42 through Column 2, lines 4). Longhenry is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with logical blocks of pixels in the level 1 cache, as Longhenry teaches, for MPEG macroblock efficiency.

Claim Rejections - 35 USC § 103

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, Jeddeloh, U.S. Patent Application Publication 2003/0070044, Longhenry et al, U.S. Patent 5,991,865, as applied to claims 1, 4

above, and in further view of Crump et al, U.S. Patent 5,860,086 and Buckelew et al, U.S. Patent 6,667,744.

10. Regarding claim 5, Olszewski, Bowles and Longhenry disclose the graphics system of claim 4, wherein the status information, logical block in the level one cache memory and which portions of the graphics data in the level one cache memory has been modified (see above).

Olszewski does not disclose comprises: a least recently used (LRU) count, wherein the LRU count indicates which has been least recently accessed. Crump teaches a least recently used (LRU) count, wherein the LRU count indicates which has been least recently accessed (Column 14, lines 24-41). The motivation for combining level one cache information tracking with LRU count indicates which has been least recently accessed is to know which data to throw away when a cache miss occurs (Column 14, line 40; Abstract). Crump is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with LRU count, as Crump teaches, for video memory efficiency.

Olszewski, Bowles and Longhenry disclose blocks and which portions of the graphics data in the level one cache memory has been modified (see above), but Olszewski does not disclose and a dirty bit [to] indicate which portions are modified. Buckelew teaches a dirty bit (Column 23, line 60 through Column 24, line 13). The motivation for combining level one cache information tracking with dirty bit is for high performance, accelerated frame buffer graphics application (Column 8, line 61 through Column 9, line 7). Buckelew is evidence that at the time

of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with dirty bit, as Buckelew teaches, for high speed frame buffer application.

Claim Rejections - 35 USC § 103

11. Claims 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, Jeddeloh, U.S. Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Buckelew et al, U.S. Patent 6,667,744.

12. Regarding claim 6, Olszewski, Bowles and Jeddeloh disclose a graphics system of claim 1, configured to output the memory requests to the memory request processor in response to control signals from the memory request processor (see above).

Olszewski does not disclose further comprising a request queue connected to the memory request processor, wherein the request queue comprises a first-in-first-out (FIFO) storage structure, wherein the request queue is configured to receive and buffer memory requests. Buckelew teaches a request queue connected to the memory request processor, wherein the request queue comprises a first-in-first-out (FIFO) storage structure, wherein the request queue is configured to receive and buffer memory requests (Column 10, lines 15-18). The motivation for combining level one cache information tracking with FIFO request queue is for high performance, accelerated frame buffer graphics application (Column 8, line 61 through Column

9, line 7). Buckelew is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with FIFO request queue, as Buckelew teaches, for high speed frame buffer application.

13. Regarding claim 8, Olszewski, Bowles and Jeddeloh disclose a graphics system of claim 1, wherein the memory connected to the RAM, wherein the memory is configured to receive and store portions of the graphics data from the RAM (see above).

Olszewski does not disclose comprises a shift register, and wherein the shift register is further configured to output graphics data serially in response to an external clock signal. Buckelew teaches comprises a shift register, and wherein the shift register is further configured to output graphics data serially in response to an external clock signal (Column 18, lines 12-20). The motivation for combining level one cache information tracking with shift register is for high performance, accelerated frame buffer graphics application (Column 8, line 61 through Column 9, line 7). Buckelew is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with shift register, as Buckelew teaches, for high speed frame buffer application.

14. Regarding claim 9, Olszewski discloses a graphics system of claim 8, further comprising a display device, wherein the display device displays images according to the graphics data (Column 3, line 37; Column 4, lines 2-3).

Claim Rejections - 35 USC § 103

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, Jeddeloh, U.S. Patent Application Publication 2003/0070044, and Buckelew et al, U.S. Patent 6,667,744, as applied to claims 1, 6 above, and in further view of Crump et al, U.S. Patent 5,860,086.

16. Regarding claim 7, Olszewski, Bowles and Jeddeloh disclose a graphics system of claim 6, wherein the array of registers is divided into two distinct sets, wherein one set of registers stores status information indicative of a current state of the level one cache (see above).

Olszewski does not disclose registers is divided into two distinct sets, and wherein the second set of registers stores status information. Bowles teaches registers is divided into two distinct sets, and wherein the second set of registers stores status information (Column 7, lines 25-50). The motivation for combining level one cache information tracking with two register sets is for reducing the cache memory access or snooping overhead (Column 1, lines 14-18). Bowles is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with register sets, as Bowles teaches, to improve cache memory efficiency.

Olszewski does not disclose the level one cache plus the predicted results of one or more memory requests pending in the request queue. Crump teaches plus the predicted results of one

or more memory requests pending in the request queue (Column 14, lines 55-65, *read ahead*). The motivation for combining level one cache information tracking with predicted results is to know which data to throw away when a cache miss occurs (Column 14, line 40; Abstract). Crump is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with predicted results, as Crump teaches, for video memory efficiency.

Claim Rejections - 35 USC § 103

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al, U.S. Patent 6,339,818, Bowles, U.S. Patent 5,796,980, Jeddeloh, U.S. Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Crump et al, U.S. Patent 5,860,086 and Longhenry et al, U.S. Patent 5,991,865.

18. Regarding claim 10, Olszewski, Bowles and Jeddeloh disclose a graphics system of claim 1, level one cache memory and store the results in the level one cache (see above).

Olszewski does not disclose wherein the memory further comprises an arithmetic logic unit (ALU) connected to the level one cache memory. Crump teaches wherein the memory further comprises an arithmetic logic unit (ALU) connected to the level one cache memory (Figure 9, elements 40a, 32a, Column 15, lines 54). The motivation for combining level one cache information tracking with ALU-cache memory is to know which data to throw away when a cache miss occurs (Column 14, line 40; Abstract). Crump is evidence that at the time of the

invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with ALU-cache memory, as Crump teaches, for video memory efficiency.

Olszewski does not disclose wherein the ALU is configured to: receive as one operand graphics data from a source external to the memory; receive as a second operand graphics data stored in the level one cache; arithmetically combine the two operands according to a function defined by an external control signal; and store the results of the arithmetic combination. Longhenry teaches receive as one operand graphics data from a source external to the memory; receive as a second operand graphics data stored in the level one cache; arithmetically combine the two operands according to a function defined by an external control signal; and store the results of the arithmetic combination (Figure 3, source A and source B, Column 7, lines 9-63). The motivation for combining level one cache information tracking with ALU operands is that multimedia decompression using vectorized real time video data and MPEG standards requires moving large monolithic chunks in blocks to achieve a greater bandwidth (Column 1, line 42 through Column 2, lines 4; Column 8, lines 15-30). Longhenry is evidence that at the time of the invention, it would have been obvious to one skilled in designing hierarchical memory graphics processing machines, to combine the benefits of level one cache information tracking, as Olszewski discloses, with ALU operands, as Longhenry teaches, for MPEG macroblock efficiency.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

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March 4, 2004

Matthew C. Bella

MATTHEW C. BELLA
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